WHAT IS CLAIMED IS:

1. An active matrix liquid crystal display element comprising:

a plurality of source lines for transmitting a video signal;

a plurality of gate lines arranged so as to intersect the plurality of source lines in a plan view, for transmitting a gate signal;

a plurality of pixels defined by the plurality of source lines and the plurality of gate lines which intersect each other and constituting an image display plane;

a pixel electrode provided for every pixel;

an opposed electrode facing the pixel electrode across a liquid crystal layer;

a storage capacitor provided for every pixel for holding a voltage applied between its corresponding pixel electrode and the opposed electrode; and

a pixel transistor provided for every pixel, having a source electrode, a drain electrode and a gate electrode which are connected to a corresponding one of the source lines, a corresponding one of the pixel electrodes and a corresponding one of the gate lines respectively, and being turned ON or OFF by the gate signal,

wherein an index B given by B = Lst/Lgd is equal to or greater than 7, where a periphery length of the storage capacitor is Lst and a periphery length of a gate electrode to pixel electrode capacitor, which is a capacitor formed between the gate electrode of the pixel transistor and the pixel electrode, is Lgd.

2. An active matrix liquid crystal display element according to claim 1, wherein the index B substantially ranges from 11 to 37.

3. An active matrix liquid crystal display element according to claim 1, wherein a periphery length Lof of the gate electrode to pixel electrode capacitor when the pixel transistor is in its non-continuity state is used as said Lgd and the index B is given by B = Lst/Lof.

4. An active matrix liquid crystal display element according to claim 1, wherein a periphery length Lon of the gate electrode to pixel electrode capacitor when the pixel transistor is in its continuity state is used as said Lgd and the index B is given by B = Lst/Lon.

5. An active matrix liquid crystal display element comprising:

a plurality of source lines for transmitting a video signal;

a plurality of gate lines arranged so as to intersect the plurality of source lines in a plan view, for transmitting a gate signal;

a plurality of pixels defined by the plurality of source lines and the plurality of gate lines which intersect each other and constituting an image display plane;

a pixel electrode provided for every pixel;

an opposed electrode facing the pixel electrode across a liquid crystal layer;

a storage capacitor provided for every pixel for holding a voltage applied between its corresponding pixel electrode and the opposed electrode; and

a pixel transistor provided for every pixel, having a source electrode, a drain electrode and a gate electrode which are connected to a corresponding one of the source lines, a corresponding one of the pixel electrodes and a corresponding one of the gate lines respectively, and being turned ON or OFF by the gate signal,

wherein an index D given by D = [Cof/(Clc + Cst + Cof)] × [(Lst + Lof)/Lof] substantially ranges from 0.6 to 1.5, where the value of capacitance between the pixel electrode and the opposed electrode which face each other across the liquid crystal layer is Clc, the capacitance value of the storage capacitor is Cst, the capacitance value of a gate electrode to pixel electrode capacitor, which is a capacitor formed between the gate electrode and the pixel electrode, when the pixel transistor is in its non-continuity state is Cof, the periphery length of the storage capacitor is Lst, and the periphery length of the gate electrode to pixel electrode capacitor when the pixel transistor is in its non-continuity state is Lof.

6. An active matrix liquid crystal display element comprising:

a plurality of source lines for transmitting a video signal;

a plurality of gate lines arranged so as to intersect the plurality of source lines in a plan view, for transmitting a gate signal;

a plurality of pixels defined by the plurality of source lines and the plurality of gate lines which intersect each other and constituting an image display plane;

a pixel electrode provided for every pixel;

an opposed electrode facing the pixel electrode across a liquid crystal layer;

a storage capacitor provided for every pixel for holding a voltage applied between its corresponding pixel electrode and the opposed electrode; and

a pixel transistor provided for every pixel, having a source electrode, a drain electrode and a gate electrode which are connected to a corresponding one of the source lines, a corresponding one of the pixel electrodes and a corresponding one of the gate lines respectively, and being turned ON or OFF by the gate signal,

wherein an index D given by D = [Con/(Clc + Cst + Con)] $\times$ [(Lst + Lon)/Lon] substantially ranges from 0.6 to 1.5, where the value of capacitance between the pixel electrode and the opposed electrode which face each other across the liquid crystal layer is Clc, the capacitance value of the storage capacitor is Cst, the capacitance value of a gate electrode to pixel electrode capacitor, which is a capacitor formed between the gate electrode and the pixel electrode, when the pixel transistor is in its continuity state is Con, the periphery length length of the storage capacitor is Lst, and the periphery length of the gate electrode to pixel electrode capacitor when the pixel transistor is in its continuity state is Lon.

7. An active matrix liquid crystal display element according to claim 1, which is a reflective type liquid crystal display element wherein the pixel electrode is composed of a reflecting film.

8. An active matrix liquid crystal display element according to claim 1, wherein at least either the capacitance value of the storage capacitor or the capacitance value of the gate electrode to pixel electrode capacitor is set according to positions along the gate lines of the image display plane, and wherein the index B is set according to said setting.

9. An active matrix liquid crystal display element according to claim 1, wherein at least a portion of the periphery of at least one of electrodes which constitute the storage capacitor has an irregular rectangular shape in a plan view.

10. An active matrix liquid crystal display element according to claim 1, wherein at least a portion of the periphery of at least one of electrodes which constitute the storage capacitor has a saw teeth shape in a plan view.

11. An active matrix liquid crystal display element according to claim 1, wherein at least one of electrodes which constitute the storage capacitor has an H-letter shape in a plan view.

12. An active matrix liquid crystal display element according to claim 1, wherein at least one of electrodes which constitute the storage capacitor has an annular shape in a plan view.

13. An active matrix liquid crystal display element according to claim 1, wherein at least one of electrodes which constitute the storage capacitor has a meander shape in a plan view.

14. An active matrix liquid crystal display element

according to claim 1, wherein at least one of electrodes which constitute the storage capacitor has a comb shape in a plan view.

15. An active matrix liquid crystal display element according to claim 1, wherein at least one of electrodes which constitute the storage capacitor is holed in a plan view.

16. An active matrix liquid crystal display element according to claim 1,

wherein the pixel transistor is placed at a corner of its corresponding pixel in a plan view,

wherein the pixel electrode occupies a large part of its corresponding pixel, with a gap between the pixel electrode and the pixel transistor, and

wherein the periphery of the gate electrode is located inside the periphery of a channel forming semiconductor within a portion of the pixel transistor which portion extends along the pixel electrode.

17. An active matrix liquid crystal display element according to claim 1,

wherein the storage capacitor is formed between a storage capacitor forming pixel electrode and a storage capacitor forming independent electrode,

the storage capacitor forming pixel electrode being connected to its corresponding pixel electrode,

the storage capacitor forming independent electrode being connected to an independent capacitance line and facing the storage capacitor forming pixel electrode across an insulating layer, and

wherein at least a portion of the periphery of the storage capacitor forming independent electrode is located inside the periphery of the storage capacitor forming pixel electrode in a plan view.

18. An active matrix liquid crystal display element according to claim 1,

wherein the ratio between the length of an edge of the pattern of a film that constitutes the gate electrode and the length of an edge of the pattern of a film that constitutes the drain electrode, which edges are among edges of patterns that constitute the periphery of the storage capacitor, is equal to the ratio between the length of an edge of the pattern of the film that constitutes the gate electrode and the length of an edge of the pattern of the film that constitutes the drain electrode, which edges are among edges of patterns that constitute the periphery of the gate electrode to pixel electrode capacitor when the pixel transistor is in its continuity state and edges of the patterns that constitute the periphery of the gate electrode to pixel electrode capacitor when the pixel transistor is in its non-continuity state.

19. An active matrix liquid crystal display comprising:

a plurality of source lines for transmitting a video signal;

a plurality of gate lines arranged so as to intersect the plurality of source lines in a plan view, for transmitting a gate signal;

a plurality of pixels defined by the plurality of source lines and the plurality of gate lines which intersect each other and constituting an image display plane;

a pixel electrode provided for every pixel;

an opposed electrode facing the pixel electrode across a liquid crystal layer;

a storage capacitor provided for every pixel for holding a voltage applied between its corresponding pixel electrode and the opposed electrode; and

a pixel transistor provided for every pixel, having a source electrode, a drain electrode and a gate electrode which are connected to a corresponding one of the source lines, a corresponding one of the pixel electrodes and a corresponding one of the gate lines respectively, and being turned ON or OFF by the gate signal,

wherein at least the voltages of the gate signal for turning the pixel transistor ON and OFF are set to values in accordance with the distribution, within the image display plane, of at least any one of the capacitance value of a liquid crystal capacitor, the capacitance value of the storage capacitor and the capacitance value of a gate electrode to pixel electrode capacitor,

the liquid crystal capacitor being a capacitor formed between the pixel electrode and the opposed electrode which face each other across the liquid crystal layer, and

the gate electrode to pixel electrode capacitor being a capacitor formed between the gate electrode of the pixel transistor and the pixel electrode.

20. An active matrix liquid crystal display according

to claim 19, wherein the center voltage of the source signal is set to a value in accordance with the distribution, within the image display plane, of at least any one of the capacitance value of the liquid crystal capacitor, the capacitance value of the storage capacitor and the capacitance value of the gate electrode to pixel electrode capacitor.

21. An active matrix liquid crystal display according to claim 19,

wherein at least the voltage values of the gate signal for turning the pixel transistor ON and OFF are set according to $[(Con + \tau\ Cof)/(Clc + Cst + Cof)] \times \alpha$, where the capacitance value of the liquid crystal capacitor is Clc; the capacitance value of the storage capacitor is Cst; the capacitance value of the gate electrode to pixel electrode capacitor when the pixel transistor is in its non-continuity state is Cof; the capacitance value of the gate electrode to pixel electrode capacitor when the pixel transistor is in its continuity state is Con; the voltage value of the gate signal for turning the pixel transistor ON is Vgh; the voltage value of the gate signal for turning the pixel transistor OFF is Vgl; the threshold voltage value of the pixel transistor is Vt; the center voltage value of the source signal is Vsc; α = Vgh - (Vsc + Vt); β = (Vsc + Vt) - Vgl; and $\tau = \beta / \alpha$.

22. An active matrix liquid crystal display according to claim 19, wherein the voltage values of the gate signal for turning the pixel transistor ON and OFF are set according to $[Cof /(Clc + Cst + Cof)] \times (Vgh - Vgl)$.